FIG. 1

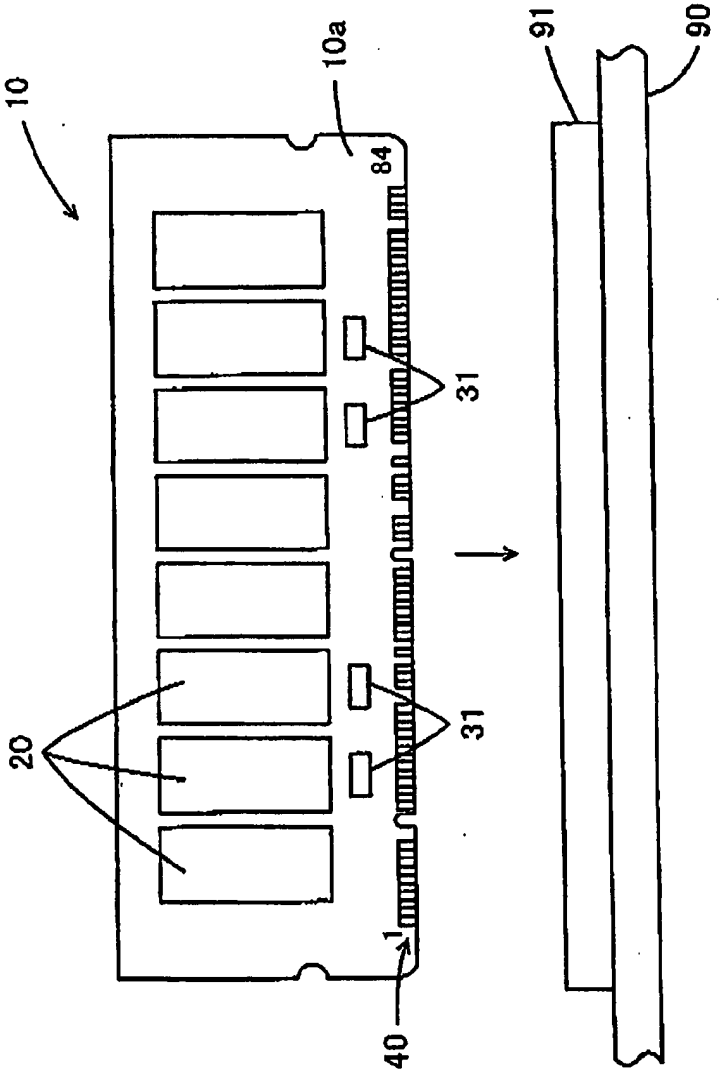

FIG. 2

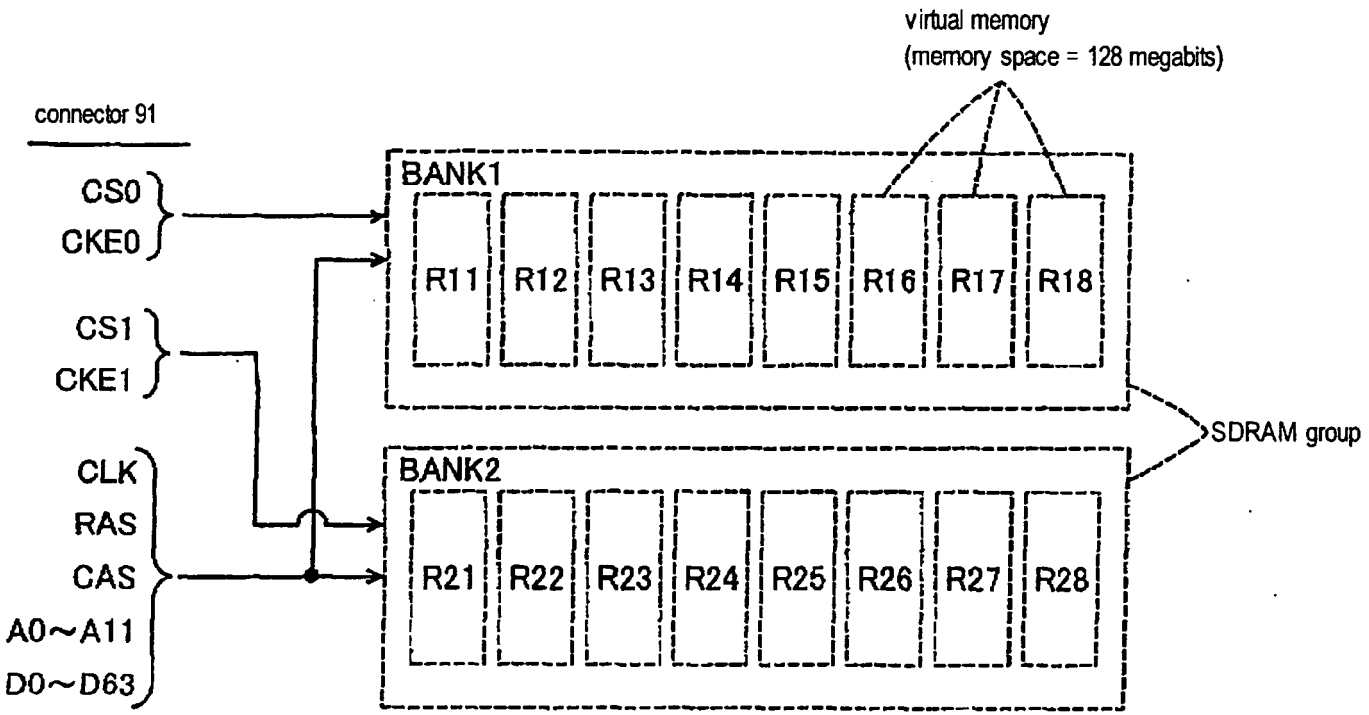
virtual memory
(memory space = 128 megabits)
connector 91
CS0
CKE0
CS1
CKE1
CLK
RAS
CAS
A0~A11
D0~D63
BANK1
R11
R12
R13
R14
R15
R16
R17
R18
BANK2
R21
R22
R23
R24
R25
R26
R27
R28
SDRAM group

FIG. 3

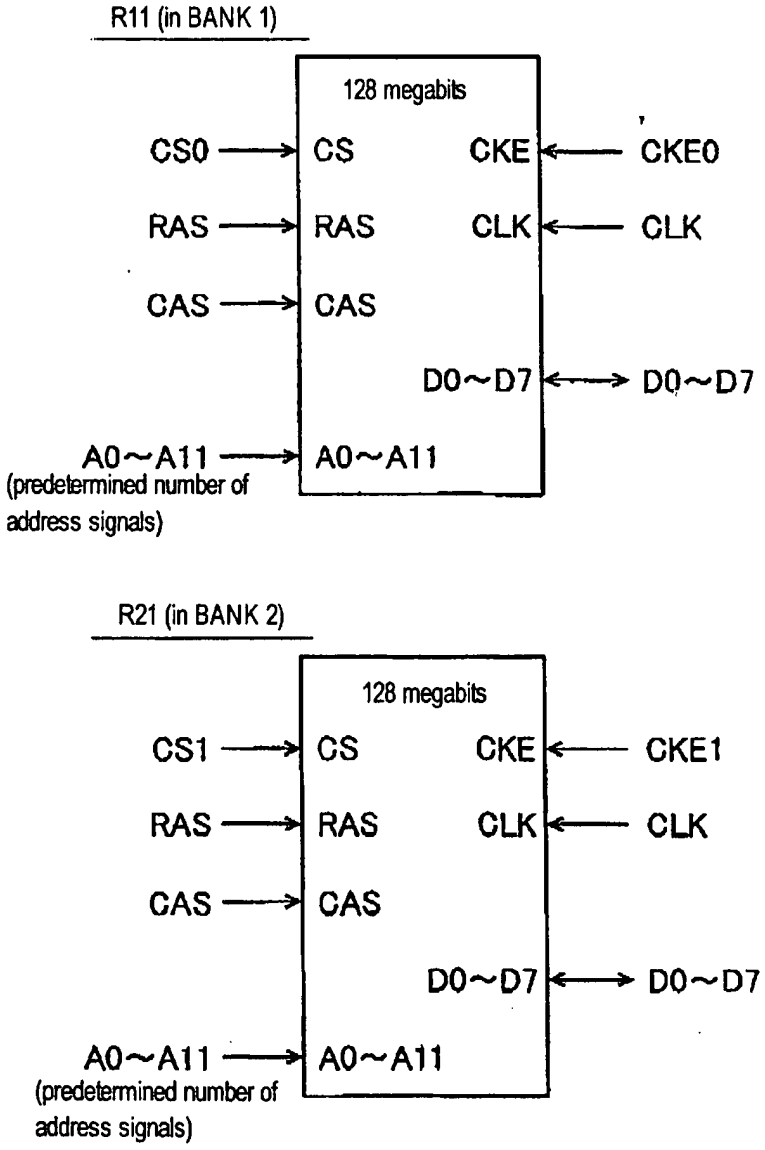
R11 (in BANK 1)
128 megabits
CS0
CS
CKE
CKE0
RAS
RAS
CLK
CLK
CAS
CAS
D0~D7
D0~D7
A0~A11
A0~A11
(predetermined number of address signals)
R21 (in BANK 2)
128 megabits
CS1
CS
CKE
CKE1
RAS
RAS
CLK
CLK
CAS
CAS
D0~D7
D0~D7
A0~A11
A0~A11
(predetermined number of address signals)

FIG.4

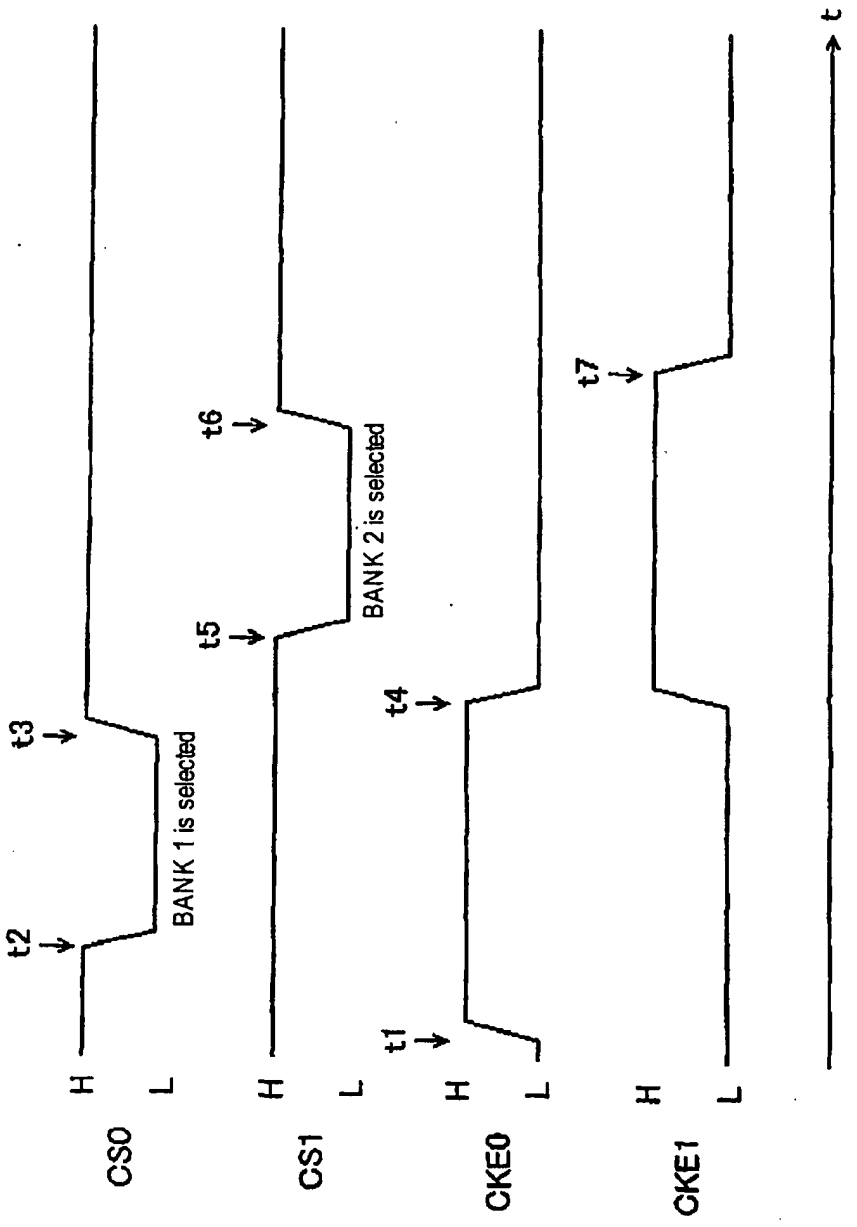
CS0
CS1
CKE0
CKE1
H
L
t1
t2
t3
t4
t5
t6
t7
BANK 1 is selected
BANK 2 is selected
t

FIG. 5

signals which can be directly inputted from a PC outputting address signals A0 to A11

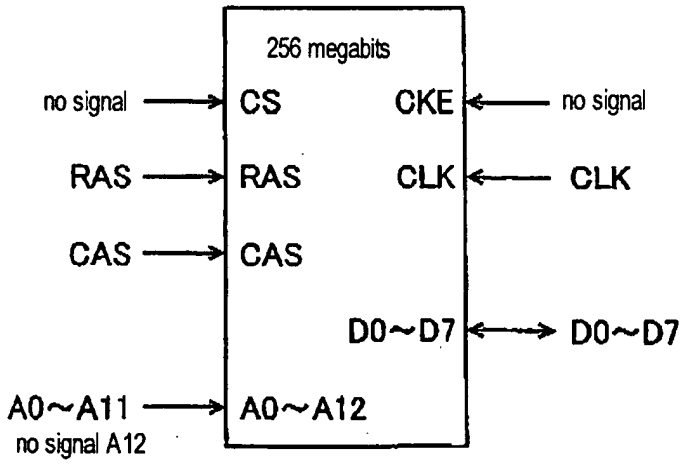

FIG. 6

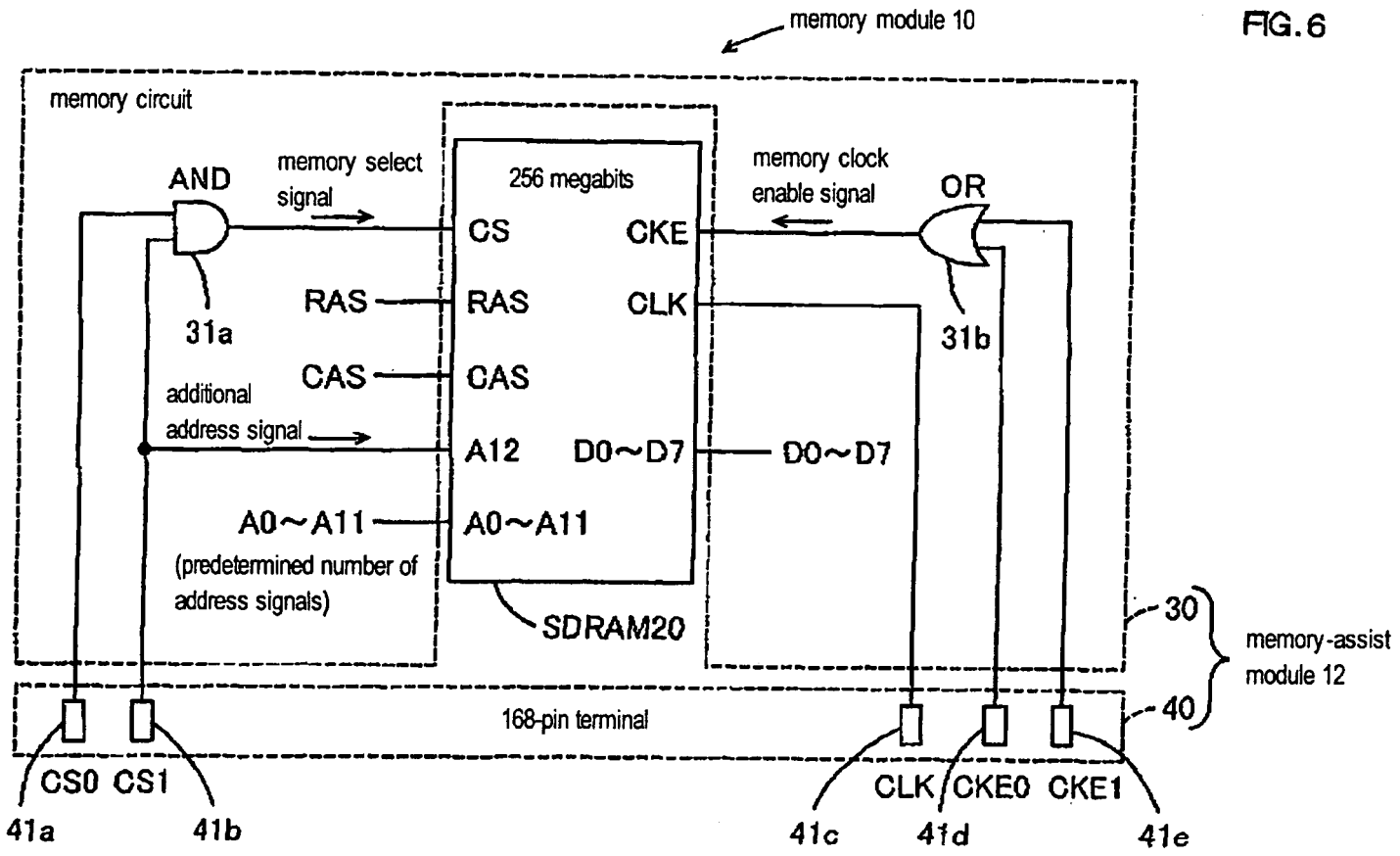
memory module 10
memory circuit
AND
memory select signal
256 megabits
memory clock enable signal
OR
CS
CKE
RAS
RAS
CLK
31a
31b
CAS
CAS
additional address signal
A12
D0~D7
D0~D7
A0~A11
A0~A11
(predetermined number of address signals)
SDRAM20
30
memory-assist module 12
168-pin terminal
40
CS0 CS1
CLK CKE0 CKE1
41a
41b
41c
41d
41e

FIG. 7

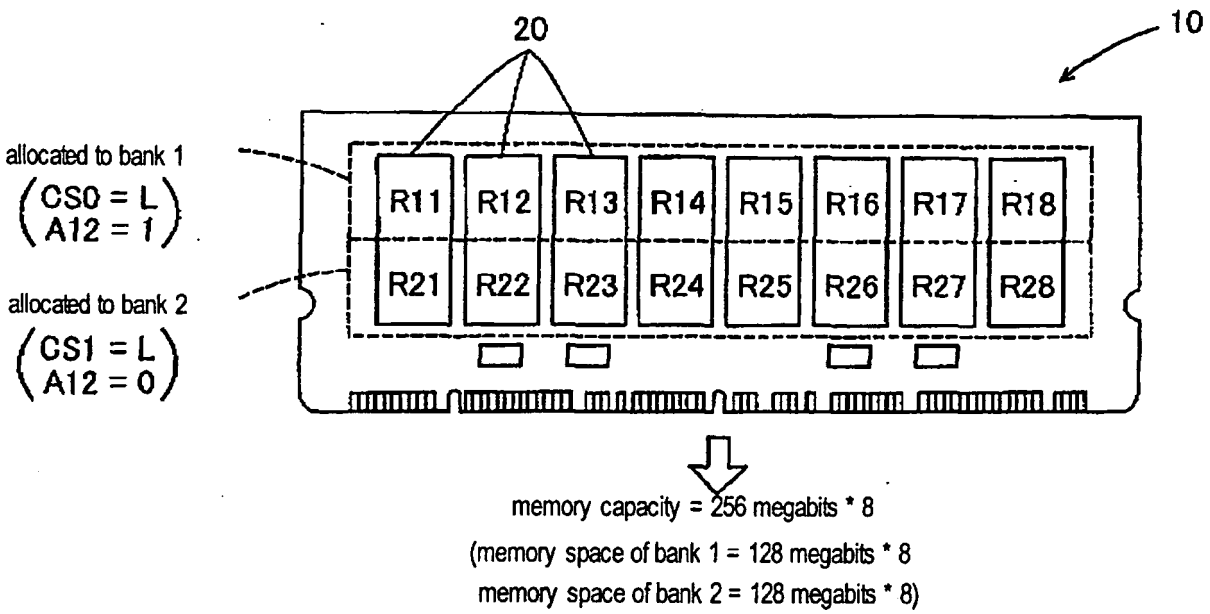
20
10
allocated to bank 1
(CS0 = L
A12 = 1)
allocated to bank 2
(CS1 = L
A12 = 0)
R11
R12
R13
R14
R15
R16
R17
R18
R21
R22
R23
R24
R25
R26
R27
R28
memory capacity = 256 megabits * 8
(memory space of bank 1 = 128 megabits * 8
memory space of bank 2 = 128 megabits * 8)

FIG.8

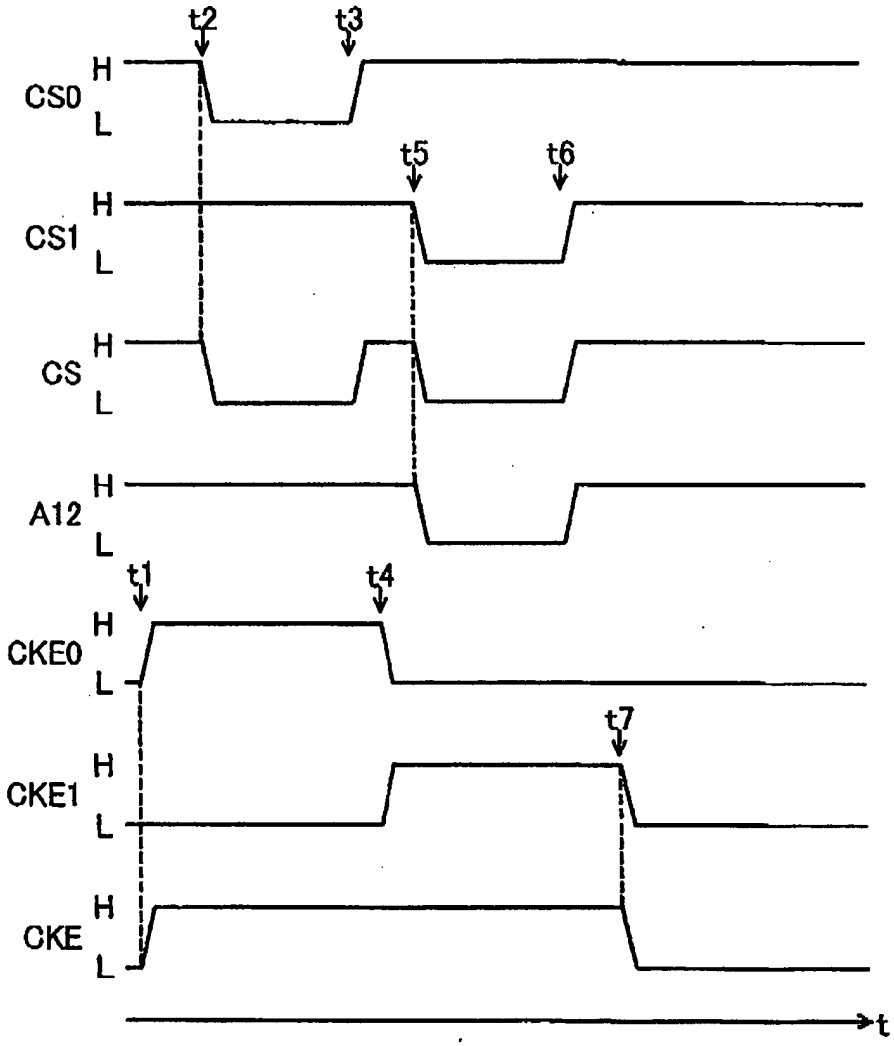
t2
t3
CS0
H
L
t5
t6
CS1
H
L
CS
H
L
A12
H
L
t1
t4
CKE0
H
L
t7
CKE1
H
L
CKE
H
L
t

FIG. 9

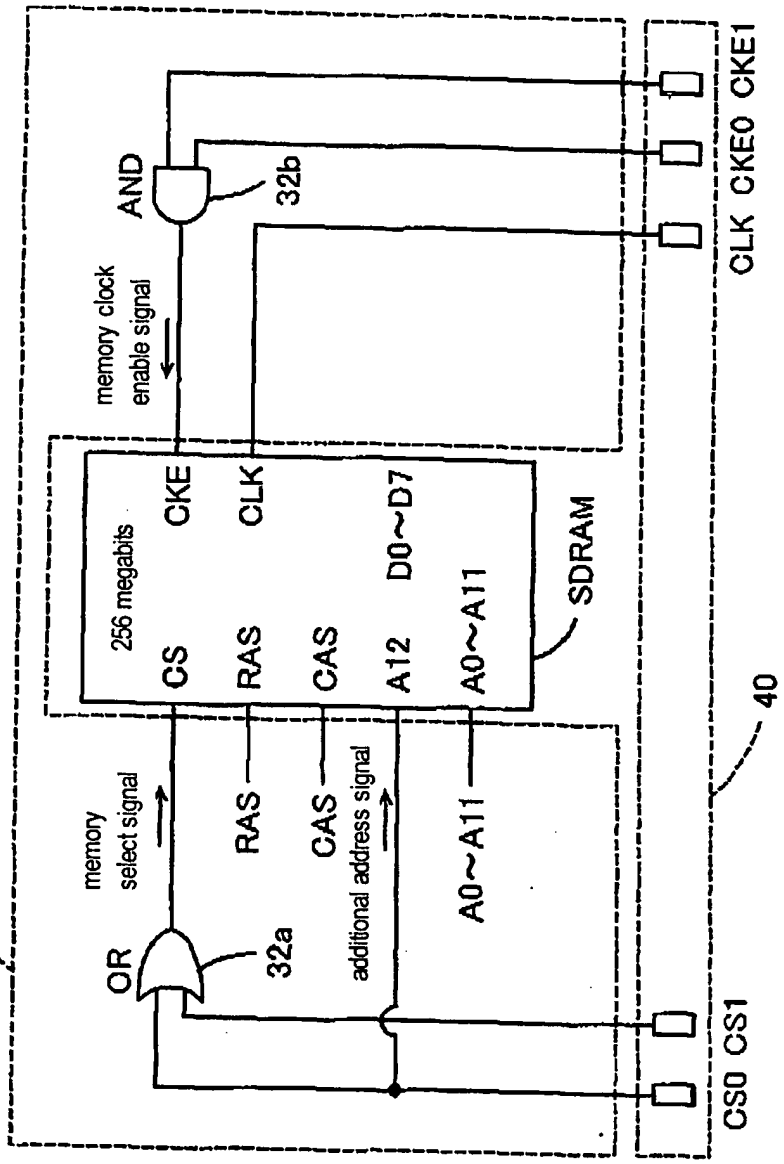
30
40
OR
32a
AND
32b
memory select signal
memory clock enable signal
additional address signal
RAS
CAS
A0~A11
CS
RAS
CAS
A12
A0~A11
CKE
CLK
D0~D7
256 megabits
SDRAM
CS0 CS1
CLK CKE0 CKE1

FIG. 10

when an additional address signal is inputted into A11 terminal

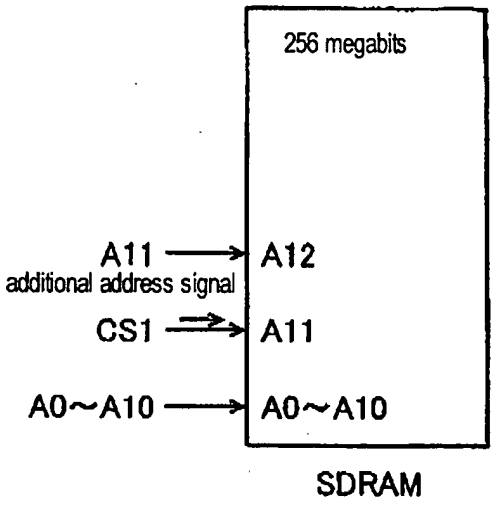

FIG. 11

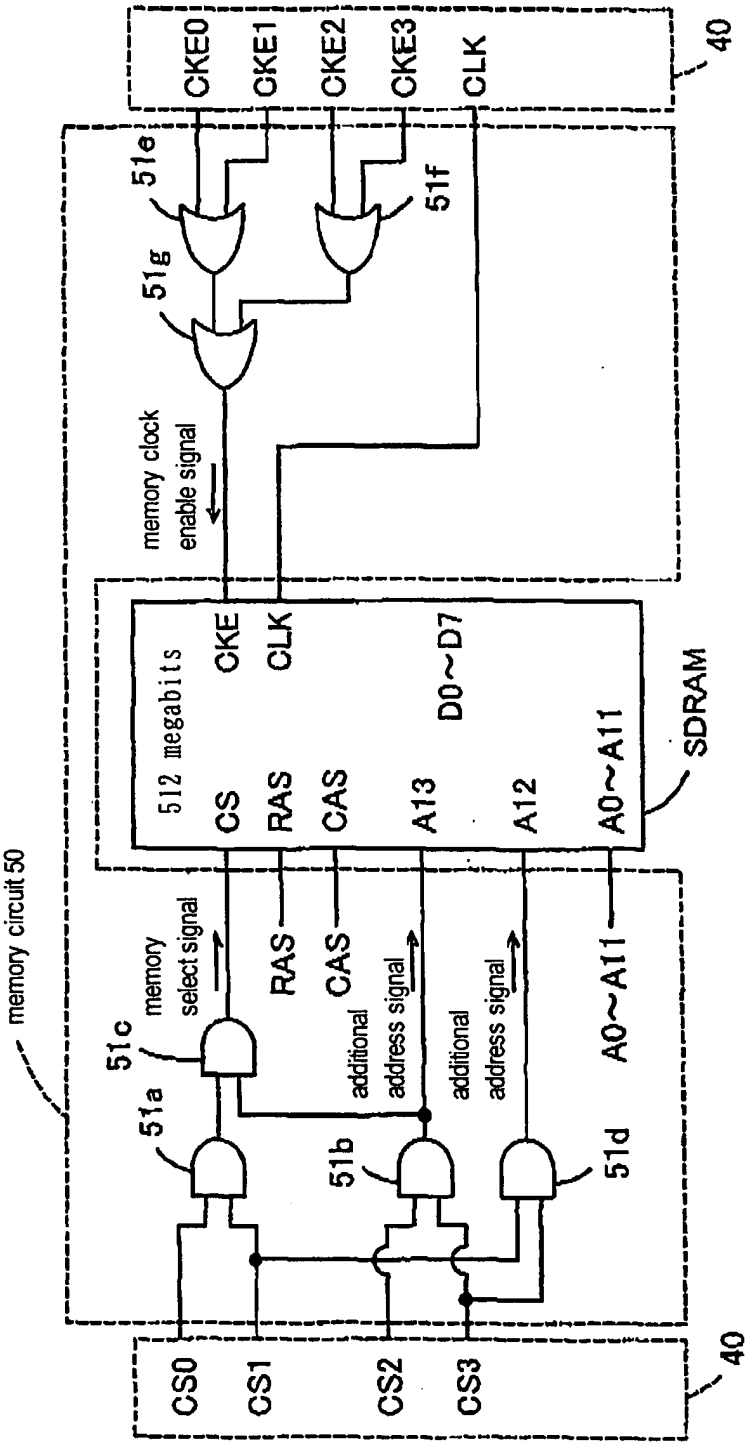
memory circuit 50
CKE0
CKE1
CKE2
CKE3
CLK
40
51e
51f
51g
memory clock enable signal
512 megabits
CKE
CLK
CS
RAS
CAS
A13
A12
D0~D7
A0~A11
SDRAM
51c
memory select signal
RAS
CAS
additional address signal
additional address signal
A0~A11
51a
51b
51d
CS0
CS1
CS2
CS3
40

FIG. 12

CS0	CS1	CS2	CS3	A13	A12
L	H	H	H	1	1
H	L	H	H	1	0
H	H	L	H	0	1
H	H	H	L	0	0